Carbon Nanotube Feedback-Gate Field-Effect Transistor: Suppressing Current Leakage and Increasing On/Off Ratio

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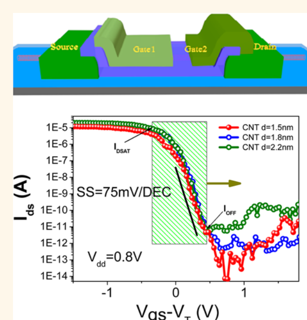
ABSTRACT Field-effect transistors (FETs) based on moderate or large diameter carbon nanotubes (CNTs) usually suffer from ambipolar behavior, large off-state current and small current on/off ratio, which are highly undesirable for digital electronics. To overcome these problems, a feedback-gate (FBG) FET structure is designed and tested. This FBG FET differs from normal top-gate FET by an extra feedback-gate, which is connected directly to the drain electrode of the FET. It is demonstrated that a FBG FET based on a semiconducting CNT with a diameter of 1.5 nm may exhibit low off-state current of about 1×10^{-13} A, high current on/off ratio of larger than 1×10^{8}, negligible drain-induced off-state leakage current, and good subthreshold swing of 75 mV/DEC even at large source-drain bias and room temperature. The FBG structure is promising for CNT FETs to meet the standard for low-static-power logic electronics applications, and could also be utilized for building FETs using other small band gap semiconductors to suppress leakage current.



KEYWORDS: carbon nanotube · field-effect transistor · gate engineering · low static power

Carbon nanotube (CNT) field-effect transistors (FETs) are among the most promising candidates for future electronics, with demonstrated superb performance due to the high carrier mobility and small intrinsic capacitance of CNTs.[1−10] Recent progresses in material synthesis on array density and selectivity[11−16] and in integrated circuit (IC) design have shown that CNT FETs move aggressively towards applications,[17−25] and presents potentially much higher speed[26−33] and lower transition power dissipation than that of silicon complementary metal-oxide-semiconductor (CMOS) devices.[19,34−36] However, static power dissipation due to leakage current in off-state in CNT FETs is hardly considered or compared with silicon devices. It is well known that speed and dynamic power consumption will profit from the scaling down of transistors,[28] while as a consequence static power consumption will increases exponentially with device scaling.[6,28,37−39] In modern silicon chips static power consumption is comparable to dynamic power, and will soon dominate in power consumption.[40,41] Suppressing static power consumption through maintaining low leakage current in transistors, for example, below 1 nA/μm,[41] has thus become a very important consideration in the development of silicon CMOS technology.

Compared with silicon transistors, CNT FETs built on moderate or large diameter CNTs typically suffer from ambipolar behavior as a result of their small band gap and thus large off-state or leakage current.[42−47] Furthermore, most high performance CNT FETs are fabricated through a doping-free process, which in a way may be regarded as Schottky barrier (SB) FETs where a SB with a height of about E_g is formed at the CNT/metal interface in off-state to prevent carriers injection.[2,48−52] In scaling down CNT FETs, the gate insulator also becomes thinner to maintain excellent electrostatic control on the channel.[37−39] As a result, the SB in off-state also becomes thinner, leading to leakage current which increases exponentially with the bias voltage between source and drain.[37−39] Although scaling down CNT FETs can improve such key device performance parameters as transconductance and gate delay, the serious degradation in off-state current or leakage during the

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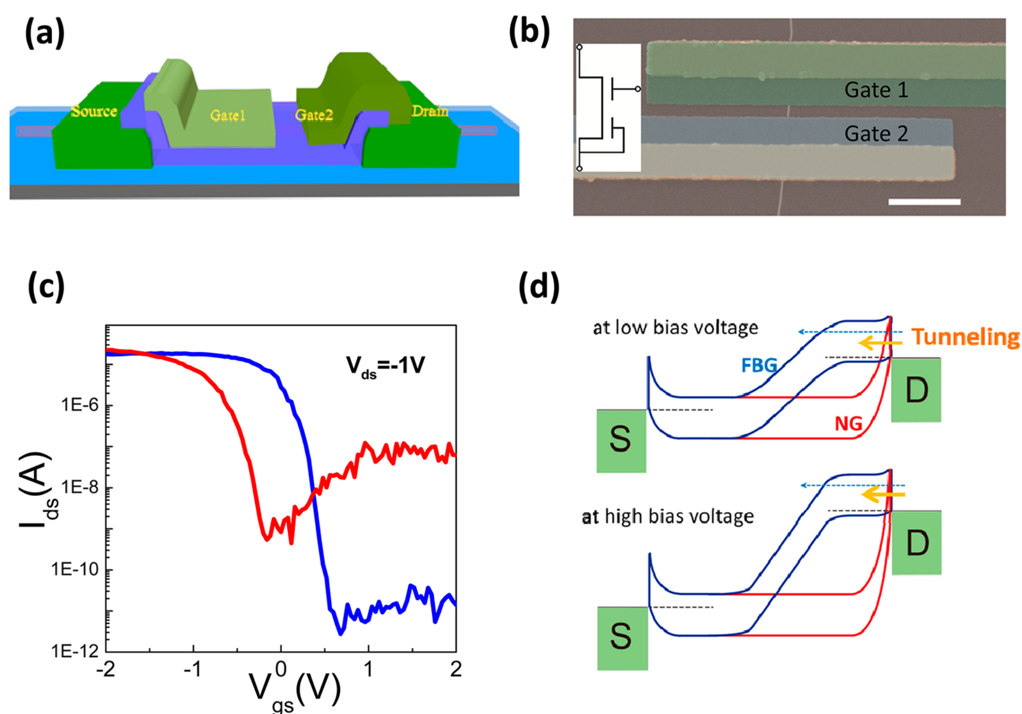

Figure 1. Carbon nanotube FBG FET. (a) Schematic of a FBG-FET. (b) Top-view SEM image of a FBG CNT FET. Inset: symbol of the FBG-FET. The scale bar is 500 nm. (c) Typical transfer characteristics of a normal (red curve) and a FBG CNT FET (blue curve) at $V_{ds} = -1$ V. The two devices are fabricated on the same CNT. (d) Schematic band structures of FBG (blue curves) and normal (red curves) CNT FETs at low bias (up) and large bias (down).

dimension scaling will eventually limit the applications of CNT FETs especially at low power dissipation electronics.

Optimization of device structure can provide efficient means for CNT FETs to suppress their ambipolar behaviors and off-state current. For example, by using MOS-like FET structure to rearrange electrostatic field near the drain electrode, ambipolar behavior of the MOS-like CNT FET may be suppressed.[53] However, air-stable MOS-like CNT FET is difficult to realize since it is difficult to achieve stable doping in graphene and CNT. Experimentally, Lin *et al.* employed a partially gated structure to realize ambipolar-to-unipolar conversion in CNT FETs through etching a trench near the drain electrode.[54] However, this structure suffers from complicated fabrication process and is not suitable for top-gate FETs since a trench is required in this device structure. Some other structures with asymmetric top gate have also been proposed to suppress off state current or ambipolar behavior in CNT FETs, but they have never been realized experimentally.[55,56]

In this work, we propose a gate structure to suppress off-state or leakage current even at large bias in CNT FETs, while maintaining their high-performance in on-state. By adding an extra feedback-gate (FBG) that is connected to the drain electrode, the width of the SB near drain is maintained. Off-state leakage current is thus significantly reduced, and ambipolar behavior is entirely suppressed. We show that this novel structured FBG CNT FET may present on/off current ratio of larger than 1×10^8, negligible drain-induced off-state leakage current, and excellent subthreshold swing even at large source-drain bias at room temperature. FBG CNT FETs built on small diameter CNTs are thus most suitable for low-static-power logic circuits. In principle, the FBG structure proposed here could also be used in FETs based on other small-bandgap semiconductors to suppress ambipolar behavior and leakage current.

RESULTS

The structure of the CNT FBG FET is depicted in Figure 1a, where two split top gates are used. Gate 1 near the source (S) is the master or control gate to switch the beneath CNT channel, and is named main gate here. Gate 2 near the drain (D) is connected to the drain electrode. This gate is used as a feedback gate to suppress tunneling current in off-state of the device, and is named feedback gate (FBG). Scanning electron microscopic (SEM) image of an as-fabricated FBG CNT FET is shown in Figure 1b, in which Gate 2 is connected to the drain electrode as illustrated by the device symbol in the inset of Figure 1b. The FBG CNT FET in Figure 1b is designed with a channel length of 500 nm, of which 200 nm is beneath the main gate and 200 nm is beneath the FBG. As a comparison, we fabricated a normal top gate FET and a FBG FET with the same channel length (500 nm) on the same CNT. Typical transfer characteristics of the two types of devices were measured at large bias and plotted together in

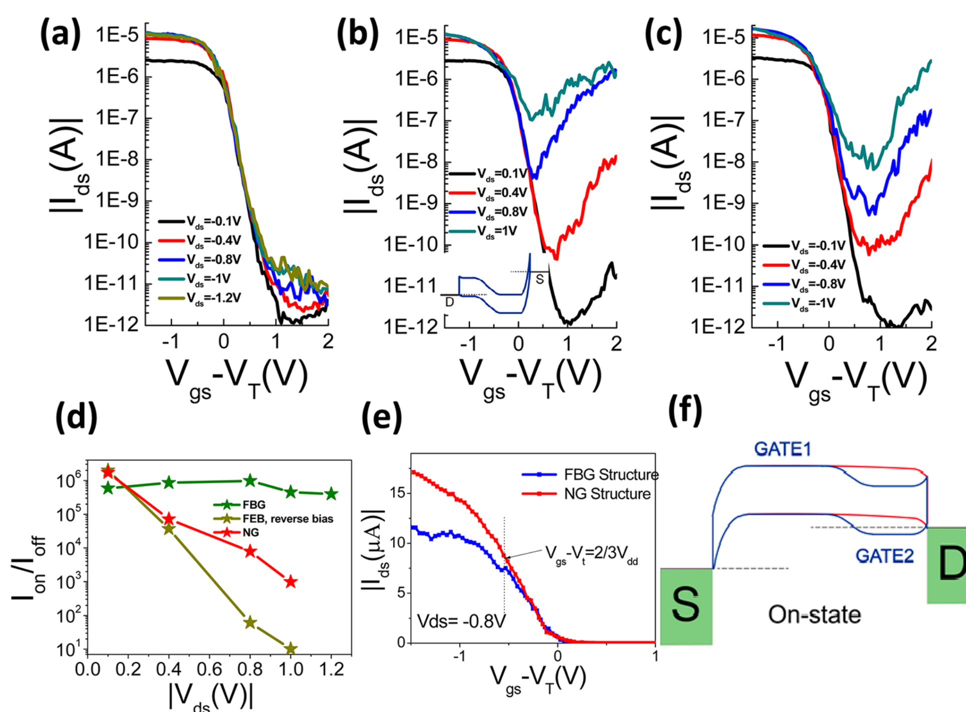

Figure 2. Comparison of FBG and NG FETs based on a CNT with a diameter of about 2.4 nm. (a) Transfer characteristics of a typical FBG CNT FET, and (b) transfer characteristics of the same device as (a) but with exchanged bias between the source and drain. (c) Transfer characteristics a normal FET on the same CNT. (d) Relation between current on/off ratio and V_{ds} for CNT FETs with different gate structures. Extracted on-state current I_{on} at $V_{gs} - V_T = -1$ V and off-state current I_{off} at $V_{gs} - V_T = +1$ V. (e) Transfer characteristic of a FBG (blue) and a NG (red) CNT FETs in linear coordinates. (f) Schematic band structures of a FBG (blue) and a NG (red) CNT FETs in their on-states.

Figure 1c. Adopting the well-developed self-aligned gate structure,[43−45] the normal top gate CNT FET shows a typical high-performance p-type field characteristic, with large on-state current of about 20 μA at bias of $V_{ds} = -1$ V and sharp on/off switching. However, the normal top-gate FET exhibits clear ambipolar behavior and large off-current of more than 1 nA (largely due to the small band gap of the CNT used here[43−45]), making it unsuitable for low-static-power applications. As shown in the band diagram (red curves in Figure 1d) of the off-state, holes are blocked by the wide SB of the CNT channel beneath the main gate, and electrons are blocked by the SB near the drain electrode at low bias. However, the SB near the drain becomes very thin at large V_{ds} or V_{gs}. Electrons from the drain can thus tunnel through the SB easily leading to large off-state or leakage current. While in the FBG FET, the energy band near the drain is maintained by the FBG which is connected to the drain, and the thickness of the SB is controlled by the FBG and may be designed to significantly suppress the off-state tunneling current even at large bias and gate voltage.

To further demonstrate the effect of gate structure on device properties, we measured transfer characteristics of a group of FETs based on a large CNT as shown in Figure 2. Figure 2a,b shows two sets of transfer characteristics from the same FBG CNT FET, but with opposite source-drain bias. And the transfer characteristics of the normal top gate (NG) CNT FET are shown in Figure 2c. Owing to the small bandgap (about 0.32 eV) of the CNT used here (with a diameter ~2.4 nm), the FET with a normal top-gate exhibits obvious ambipolar behavior with obvious leakage (tunneling) current, and the leakage current increases rapidly with increasing bias V_{ds} (Figure 2c). As a result, the current on/off ratio declines to become less than 10^3 at large bias of −1.0 V, and the minimum off-state current is as large as 10 nA. Such a large off-state current and low on/off current ratio, which are typical for top-gated CNT FETs with well scaled structure,[42−47] suggests that FETs built on large diameter CNTs with normal top gate are not suitable for low-static-power applications in large scale integrated circuits. While for the FBG FET fabricated on the same CNT, ambipolar behavior is significantly suppressed even at large bias of up to −1.2 V (Figure 2a), with an on/off current ratio of larger than 10^6 even at $V_{ds} = -1.2$ V. Under reverse V_{ds} bias (or when S and D electrodes are interchanged), the potential barrier near drain for block electron tunneling in off-state becomes a regular SB. The thickness of the SB decreases with increasing bias, leading to a large tunneling or leakage current (inset of Figure 2b). The contrast experiments further verify that the main act of the FBG is to clamp the energy band or maintain potential barrier near the drain electrode to suppress tunneling current in off state.

To demonstrate the effect of the novel FBG structure quantitatively, V_{ds} dependent I_{on}/I_{off} ratio is plotted in

Figure 2d for all three types of FETs as shown in Figure 2a–c, in which I_{on} and I_{off} at certain bias voltage are defined as the current at $V_{gs} - V_T = -1$ V and $V_{gs} - V_T = +1$ V, respectively. The I_{on}/I_{off} ratio for both normal top gate FET and reverse biased FBG FET is seen to be larger than that of the FBG FET at small bias with $V_{ds} = -0.1$ V, since the on-state current in normal top-gate FET is lightly larger than that of FBG FET. With increasing V_{ds}, I_{on}/I_{off} ratio decreases rapidly with bias in normal top gate FET and reverse biased FBG FET, suggesting that tunneling current near the drain dominates the current in off state. In a FBG FET, since a wide potential barrier exists near the drain electrode, tunneling current is significantly suppressed leading to a V_{ds} independent I_{off}. Therefore, I_{on}/I_{off} ratio in the FBG FET remains at about 10^6 with increasing V_{ds} even up to -1.2 V.

We noted earlier when discussing Figure 2d that at low bias, I_{on}/I_{off} ratio of the FBG FET is lower than that of normal FET. This is because I_{on} in the FBG FET is smaller. As a comparison, the on-state currents of the two types FETs are plotted in Figure 2e, and it is obviously that the on-state current is also suppressed to certain degree in the FBG FET. The clamping barrier near the drain electrode does not only prevent electrons from tunneling into the channel in off-state, but also constrains the on-state current. As shown in the on-state band diagram of Figure 2f, the channel potential under gate 2 is largely fixed by the Fermi level of the drain electrode, and may become a barrier for hole transport when the channel potential under gate 1 is higher than that under gate 2. As a result, on-state current is degraded in FBG FET at sufficiently large net gate voltage ($V_{gs} - V_T$). Therefore, current in FBG FET is almost equal to that of normal FET at small V_{gs}, but becomes smaller with increasing $|V_{gs}|$ as shown in Figure 2e. It is well-known that suppression of on-state current may degrade speed of the device, but at small bias regime this degradation is negligible. It should be noted that in practical applications the maximum net gate voltage ($V_{gs} - V_T$) is only about 2/3 V_{dd},[28] which limits the maximum potential difference between the channel under gate 1 and that under gate 2. For example, there exists almost not obvious current degradation when a FBG FET works at $V_{gs} - V_T = 2/3 \times 0.8$ V (Figure 2e). Therefore, the FBG structure proposed here efficiently suppresses the ambipolar behavior and off-state leakage current of a CNT device, while does not degrade its on-state current significantly.

Subthreshold swing (SS) is another important device parameter for characterizing switch performance of a FET, and keeping low SS at large bias is necessary for the design of a good FET. We measured transfer characteristics of a FBG FET fabricated on a CNT with a diameter of 2.2 nm, showing clearly unipolar behavior for a wide bias range between -0.1 V and -2 V (Figure 3a). Figure 3b shows that SS remains at a low value of around 75 mV/DEC in the full bias range, suggesting that the main gate can efficiently control the channel of the FBG FET even at large bias. Meanwhile I_{on}/I_{off} ratio remains high at above 10^6 even as V_{ds} increases up to -1.5 V as shown in Figure 3b. The slight degradation of I_{on}/I_{off} ratio at $V_{ds} = -2.0$ V is due to decreased I_{on} (inset in Figure 3a) originated from increasing optical phonon scattering at large bias. The excellent gate control is benefitted from the vertical scaling of FET, *i.e.*, using 10 nm HfO_2 as gate insulator, and the outstanding off-state behavior is sustained even at large bias of -2 V. However, ambipolar behavior and leakage current with such high-κ gate insulator are not negligible in normal CNT FETs, so FBG structure makes the FBG FET possible to have more aggressive vertical scaling than normal FET.

We now consider the effect of the FBG length on the performance of a CNT FBG FET. Figure 3c shows the scaling behavior of a group of FBG FETs which were fabricated on a CNT with a diameter of 2.2 nm. While the FBG length is scaled from 200 to 0 nm, the channel length and control gate length of these devices are fixed at 500 and 200 nm, respectively. It is obviously that off-state current increases with decreasing FBG gate length since the clamped barrier near drain becomes thinner. However, the device remains basically unipolar with small off-state current even when FBG length decreases to zero. The off-state current suppression at the FET with zero FBG length in Figure 3c comes from partial placement of the main gate between the drain and source,[54] which is similar to a MOS like CNT FET but with an asymmetric top gate. While the shrinkage of FBG length leads to a slight decrease of peak transconductance G_m as shown in Figure 3d owing to the increased ungated channel segment. It should be noted that the FBG device structure discussed in this work is unlikely to be used for scaling down CNT FET down to sub 100 nm regime, owing to the use of two split gates with non-self-aligned process. However, this does not mean that the FBG FETs cannot be scaled further down. In fact some well-designed self-aligned gate structures can give excellent scaling performance for FBG FETs. As an example, Figure S1 in the Supporting Information illustrates a process that could be used for fabricating sub-50 nm FBG transistors through a two-step self-aligned process.

The choice of metal for FBG electrode also affects the performance of FBG FET. Two FETs are fabricated with the same geometry and on the same CNT, but different metals (Pd and Al) are used as the FBG electrodes. Transfer characteristics of the two devices are shown in Figure 3e. It is seen that the Pd-FBG FET presents more efficient off-state current suppression than that of the Al-FBG FET. We note that the intrinsic work function of a semiconducting CNT is around 4.5 eV, which is lower than that of Pd (5.12 eV) but higher than Al (4.28 eV).

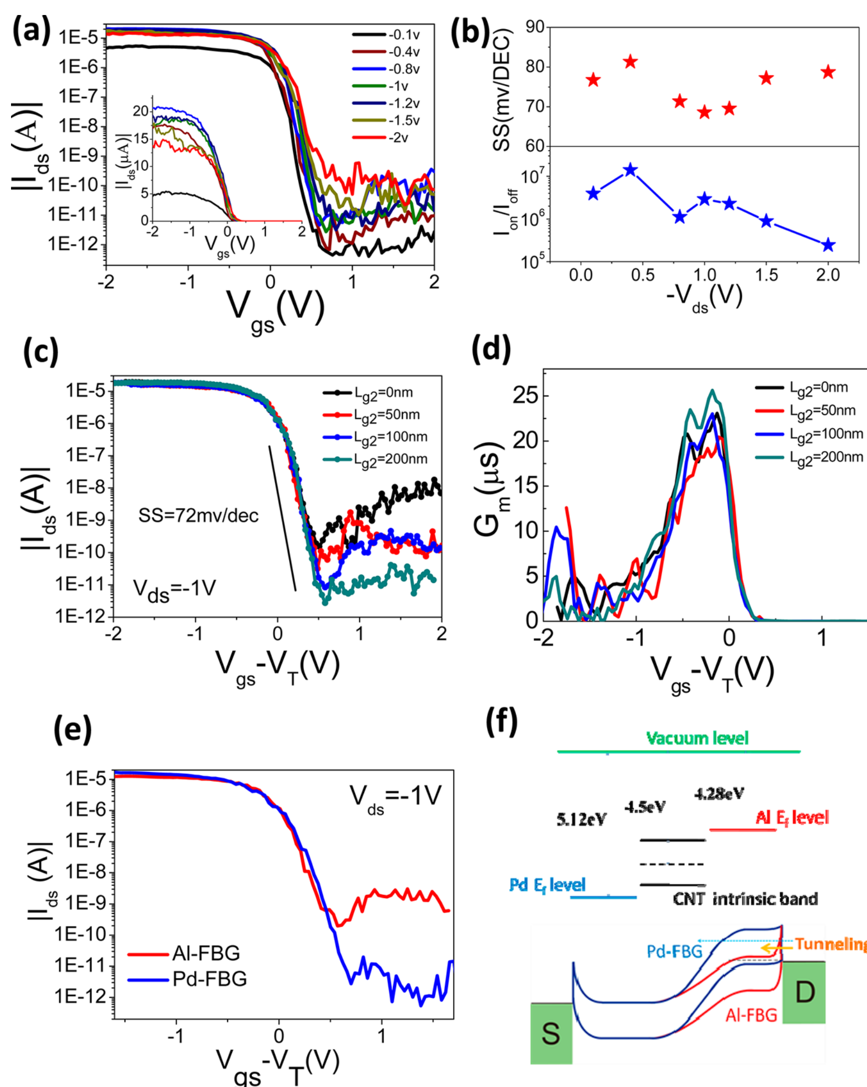

Figure 3. Performance characteristics of FBG FETs. (a) Transfer characteristics of a FBG CNT FET at bias ranged up to −2 V. Inset: the same transfer curves at linear coordinate. (b) Depedence of subthreshold swing and current on/off ratio on bias. I_{on} are extracted at $V_{gs} - V_T = -1$ V and I_{off} at $V_{gs} - V_T = +1$ V from the transfer characteristics of (a). (c) Transfer characteristics of FBG FETs with feedback gate length ranged from 200 to 0 nm. The channel length and control gate length are fixed at 500 and 200 nm, respectively, and at bias of $V_{ds} = -1$ V. (d) Gate voltage-dependent transconductances, as extracted from (c). (e) Transfer characteristics of two FBG FETs for Pd-gate (blue) and Al-gate (red) at large bias $V_{ds} = -1$ V. (f) Schematic band diagram for Pd-FBG (blue) and Al-FBG (red) CNT FET in off state.

As shown in the band diagram of Figure 3f, Pd-FBG pushes the Fermi level E_F of the CNT channel toward the valence band (inducing hole in the channel under FBG, hole-enhanced), while Al-FBG pushes E_F toward the conductance band (inducing electron in the channel under FBG). The combination of Pd-FBG and Pd-Drain thus results in a wide rectangular barrier near the Pd-drain, preventing electrons from tunneling into the channel in off-state. This situation is in contrast with the sharp barrier associated with the combination of Al-FBG and Pd-Drain, which results in a larger tunneling or leakage current. Therefore, the metal for FBG electrode should be chosen carefully, and the general rule is to choice high work-function metal for p-type FET and low work-function metal for n-type FET.

Large current on/off ratio and ultralow off-state current are of crucial important for designing good transistors in order to construct ICs with low static power consumption. It is well-known that static power consumption is comparable to dynamic power in modern silicon chips or even become dominating in the future.[41] Therefore, off-state current density is usually used as a key parameter to characterize the power consumption of a device in modern ICs.[41,42] It is well-known that FETs built on semiconducting CNTs with smaller diameter present smaller leakage current owing to their larger band gap. Therefore, we measured transfer characteristics of a FBG FET fabricated on a CNT with a diameter of 1.5 nm, showing clearly unipolar behavior (Figure 4a). It is worth noting that the minimum off-state current is as small as 10^{-13} A, which

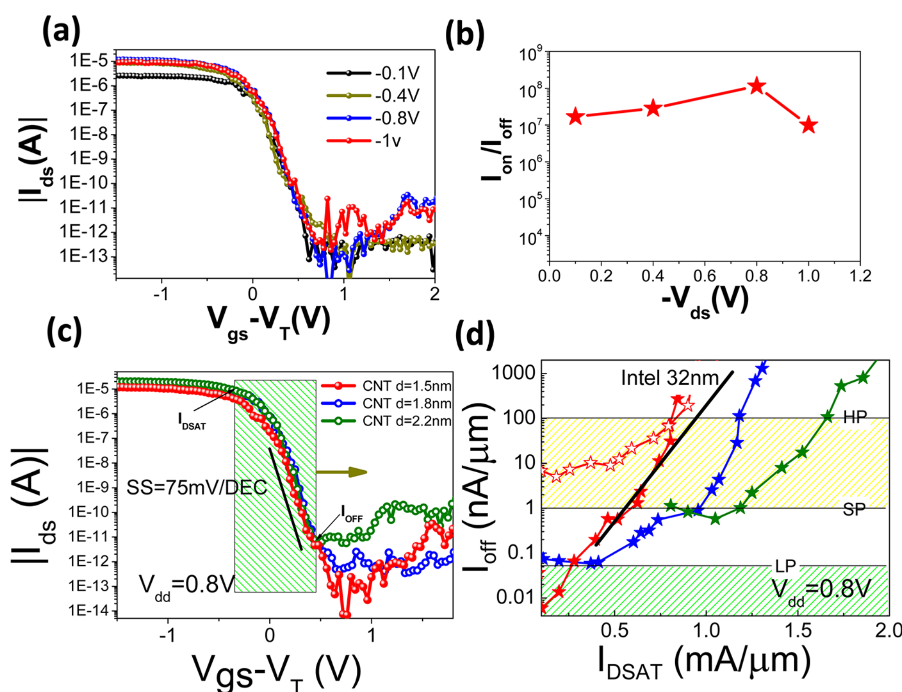

Figure 4. Low standby power characteristics of carbon nanotube FBG FET. (a) Transfer characteristic a FBG FET based on a CNT with diameter of 1.5 nm, and (b) current on/off ratio for different V_{ds}. I_{on} is extracted at $V_{gs} - V_T = -1$ V and I_{off} at $V_{gs} - V_T = +1$ V from the transfer characteristics of (a). (c) Transfer characteristics of three FBG FETs on CNTs with different diameters of 1.5, 1.8, and 2.2 nm, respectively, at bias of $V_{ds} = -0.8$ V. (d) Leakage characteristics of three FBG FETs based on different CNTs with diameter of about 1.5 nm (red solid stars), 1.8 nm (blue stars), and 2.2 nm (olive stars), while the data of normal gate FET (on 1.5 nm CNT, red hollow stars), 32 nm (black line) node silicon PMOS FET of Intel are used as references. The CNT FETs were assumed to be constructed on aligned array with density of 125 CNTs/μm.

is comparable to the noise level of our measurement system. The current on/off ratio for this device can be as large as about 10^8 at large bias (-0.8 V) at room temperature (shown in Figure 4b), which is much larger than that of all published top-gated CNT FETs.[42−47]

To further highlight the effect of diameter of CNTs, we compared FBG FETs on three different CNTs with diameters of 1.5, 1.8, and 2.2 nm, respectively, and typical transfer characteristics at large $V_{ds} = -0.8$ V are shown in Figure 4c. The FBG FET on 1.5 nm CNT presents large current on/off ratio up to 10^8 at bias of -0.8 V. For the FBG FET built on the larger CNT with diameter of 2.2 nm, the current on/off ratio of the device remains larger than 10^6 at large bias (-0.8 V), and obviously with larger on-state current than that built on the smaller CNT with a diameter of 1.5 or 1.8 nm. All three FETs show SS well about 75 mV/DEC, suggesting that FBG structure can provide excellent gate control for CNTs with wide diameter range.

It is well established that both on- and off-state currents for CNT FET with normal top gate increase with increasing diameter of semiconducting CNT, which is also true for the results shown in Figure 4c for FBG FETs. In modern silicon based IC technology, system-on-chip (SOC) has become the mainstream IC manufacturing trend, which integrates several functional circuit blocks including high performance cores and low standby power always-on circuitry to achieve complex function and balance the speed and power. Different leakage levels of transistors on a SOC chip are achieved by adopting multithreshold technology.[57] Two main types of transistors are needed in high-speed logic cores, high performance (HP) with a leakage at 100 nA/μm and standard performance (SP) with a leakage at 1 nA/μm. The battery-powered always-on circuitry has an even more rigorous standard on leakage, *i.e.*, below 50 pA/μm, and requires more careful design of transistors to work at low power (LP). In principle, different CNT FETs can be used for different IC applications according to the diameter of the CNT used, *i.e.*, FETs based on large diameter CNTs may be used for high-speed ICs, while FETs based on small CNTs may be used for low-power applications. To benchmark the performance and static power dissipation of CNT FETs, I_{off} and I_{DSAT} are defined in a fixed voltage range, for example, 0.8 V as in Figure 4c.

By moving the voltage window of V_{dd} (0.8 V) along a transfer characteristic, I_{off}−I_{DSAT} (for definition see Figure 4c) relation for a device can then be obtained and used to estimate the speed and static power performance of the device. I_{off}−I_{DSAT} curves for four types of CNT FETs with different diameters and gate structures are shown in Figure 4d, in which the current has been normalized assuming using an aligned uniform CNT array with a density of 125 CNTs/μm. Three conclusions can be drawn from the information presented in Figure 4d. (1) CNT FBG FETs can be classified for different applications according to the

diameter of the CNTs used. These correspond to the three main types of transistors required in modern ICs according to static power, *i.e.*, devices for HP applications with leakage at 100 nA/μm, for SP applications with leakage at 1 nA/μm, and for LP applications with leakage under 100 pA/μm.[57] According to the above standards, FBG FETs based on CNTs with diameters larger than 1.5 nm are suitable for HP and SP applications, while FBG FETs based on CNTs with diameters smaller than 1.5 nm can meet the requirements for LP applications. (2) FBG structure significantly reduces static power of CNT FETs without lowering their speed. While leakage in a normal FET based on a 1.5 nm CNT is much higher than the standard of LP applications (Figure 4d), the FBG FET based on the same CNT presents much lower I_{off} (as low as 30 pA/μm) than the normal FET, and can extend CNT FET to low power applications at low bias of less than 0.4 V. (3) CNT FBG FETs may present significant advantages on speed than silicon devices with similar static power dissipation, since FBG FETs based on large diameter CNTs (1.8 and 2.2 nm) present much higher I_{DSAT} (at same I_{off}) than that of the 32 nm silicon PMOS device (Figure 4d). Therefore, the novel FBG structure for CNT FETs can significant reduce static power while maintain the original speed advantage, and is thus promising for pushing CNT FET into LP applications.

Last but not the least, while we only discussed CNT based FETs here, the FBG structure may be readily used in devices based on other small bandgap semiconductors, such as InAs film (or nanowires or bulk),[58] core−shell Ge/Si nanowire[59] and grapheme nanoribbons[60] with high carrier mobility for building high-speed transistors, where ambipolar behavior and large off-current originated from the small bandgap are highly undesirable for applications of these transistors in future ICs. In principle, the FBG structure discussed in this work may be utilized to build FETs based on these small bandgap semiconductors to suppress leakage current.

CONCLUSION

We have developed a feedback-gate structure to suppress off-state current in CNT FETs while maintaining their high-performance in on-state. In a FBG FET, the width of the potential barrier near the drain is largely fixed by the feedback gate, which suppresses significantly the undesired ambipolar behavior of the FET and thus off-state leakage current. The novel FBG CNT FETs present on/off current ratio of larger than 1×10^8, low off-state current of smaller than 1×10^{-13}A, negligible drain-induced off-state leakage current and excellent subthreshold swing even at large source-drain bias at room temperature. The FBG structured CNT FETs are demonstrated to be promising to meet the standard of low-static-power logic ICs, and the FBG structure may in principle be used for building FETs based on other small-bandgap semiconductors to suppress leakage current.

METHODS

Single-wall CNTs used in this work were directionally grown on a silicon substrate, and semiconducting single-walled CNTs were identified *via* field-effect measurements using the substrate as the back gate. Diameters of the selected semiconducting CNTs were measured by using atom-force microscopy (AFM) at first. Source and drain electrodes were formed through patterning using electron-beam lithography (EBL) followed by depositing 30 nm Pd film using electron-beam evaporator (EBE) and a standard lift-off process, and then 8 nm HfO_2 gate insulator with dielectric constant of about 15 was grown by atomic layer deposition (ALD) at 90 °C. Control gate electrode with 10 nm Pd film was formed through EBL and EBE, while feedback gate electrode was formed using 20 nm Pd or Al through another process combination of EBL and EBE. FBG and drain electrode were connected by local metal interconnection. All electric measurements were carried out by probe station in air using Keithley 4200 semiconductor analyzer.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Process flow for self-aligned FBG FET. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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